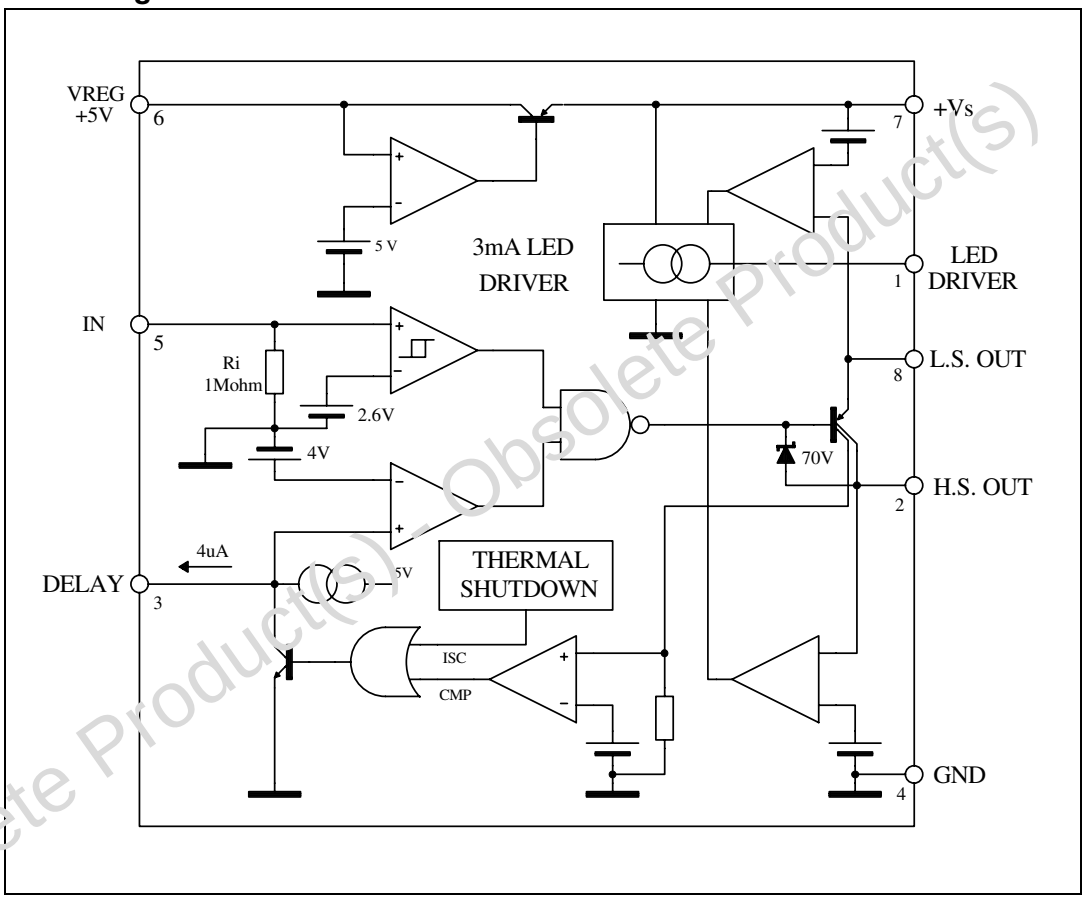
AN495
Application note

Effective filtering of TDE1707

Introduction

The TDE1707 is an industrial I.P.S. (intelligent power switch). Dedicated to proximity detectors, it can deliver up to 0.5 A to a "configurable" load (load to battery or load to ground configuration); see block diagram below.

Block diagram



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1 Effective filtering

On the application circuit (*Figure 1.*) of the TDE1707 Data-Sheet, the use of filter capacitors is recommended on both :

- The power supply (+Vs pin 7).
- The +5 V regulated voltage (Vreg pin 6).
  - To understand the function of the Vreg capacitor, it is necessary to consider that the Vreg pin makes available a regulated voltage that can be used to supply external circuits (typically proximity detectors); but the TDE1707 itself, always uses the Vreg to supply most of its internal circuits (see*: Block diagram*). Internally to the TDE1707, Vreg supplies all the functional blocks, except the output power transistor (and the Driver-Led, when the Led is connected as in "load to GND. configuration").
  - In the real application, the TDE1707 and associated circuitry, can be significantly far away from the power supply and the long connection wires will act as a serial inductance.

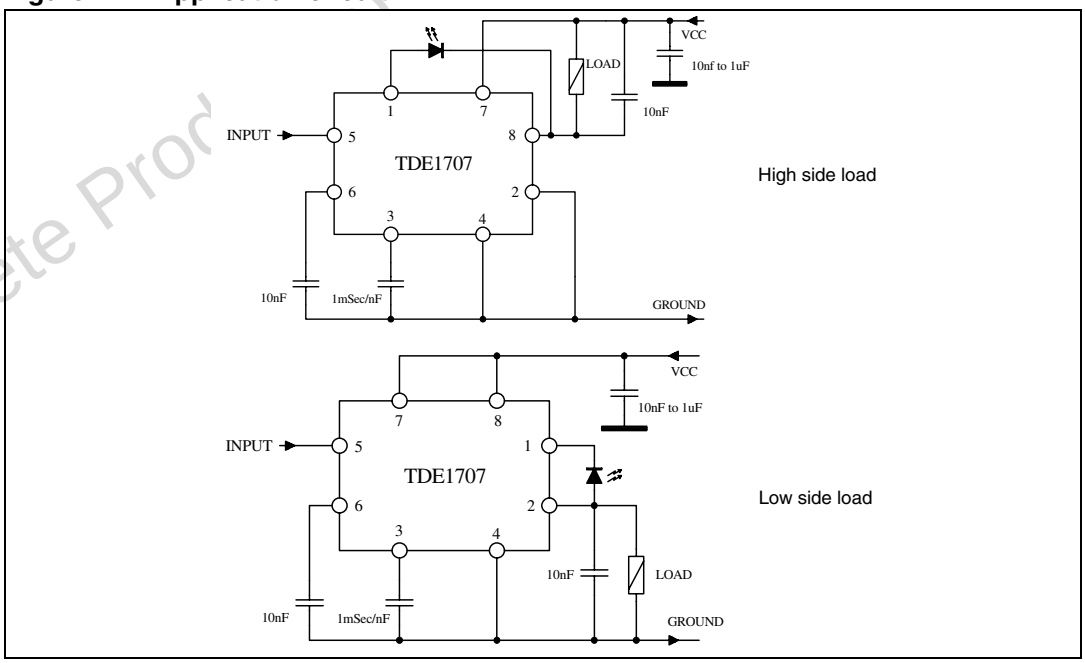
At power on, or at the turn-on of the power transistor, or in coincidence to load variations, this inductance will react to the current variations with wide voltage variations. In proximity sensor applications, for space reasons, the size of the filtering capacitors has to be reduced as much as possible.

The voltage oscillation can induce two kind of problems in the circuit:

1. Overvoltage on the +Vs pin, connected to the +24V bus, that can exceed the TDE1707 rated limit.
2. Disturbances inside the circuit (TDE1707), because the noise immunity level is exceeded with disruption of the input/output function.

Filtering the overvoltage on the +Vs is possible

Figure 1. Application circuit



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only by an external capacitance between +Vs (pin7) and Ground (pin4) to limit voltage spikes at the device's rated values.

Immunity problems in the circuit are essentially related to the +5 V Vreg filtering, because the noise on this voltage can induce errors in the low-voltage circuits.

The best solution, to avoid immunity problems, is to put the filter capacitor between Vreg and Ground even if the Vreg dees not supply any external circuits. Compared to the +Vs capacitor filtering effect, that also improves the immunity, the Vreg capacitor offers two advantages:

1. The capacitive value can be significantly lower, for the same filtering effect, because the Vreg filter does not have to sustain the load current variations.
2. The nominal voltage of the capacitor is lower (6 V instead of 25-50), so that the phisical size of the capacitor is also smaller.

The higher effectiveness of filtering Vreg instead of +Vs is always evident. On average, in a typical application, a capacitor put on Vreg can, with the same filtering effectiveness of a capacitor on +Vs, be 20 times smaller in value.

Nonetheless, a capacitor on +Vs, although not of high value, is recommended. Its value shall be adapted in accordance to the equivalent inductance of the supply connections and of the value of the load.

For instance, the values used in the test circuit (*Figure 2.*) :

- 325 µH are too high to be found in pratice.
- 4.7nF on +Vs are barely sufficient with 325 µH (with 325 µH, 10nF would be preferable).
- 4.7nF on Vreg are sufficient in most of the pratical cases.
- Using the test circuit shown in *Figure 2.*, with the input trigger of the TDE1707 in pulsed mode, the effect of the capacitor un Vreg (pin 6) can be noted in diagrams *Figure 3.* and *Figure 4.*:
  - *Figure 3.* shows the voltage, on +Vs (Ch1) and Vreg (Ch2), at turn-on and turn-off edges, without the filter capacitor on pin 6.
  - *Figure 4.* shows the same signals but with 4.7 nF capacitor connected between Vreg (pin 6) and Ground.

The improvement of the immunity level and the low values of the capacitors makes the suggested filtering solution the best for proximity detector application.

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Figure 2. Test circuit

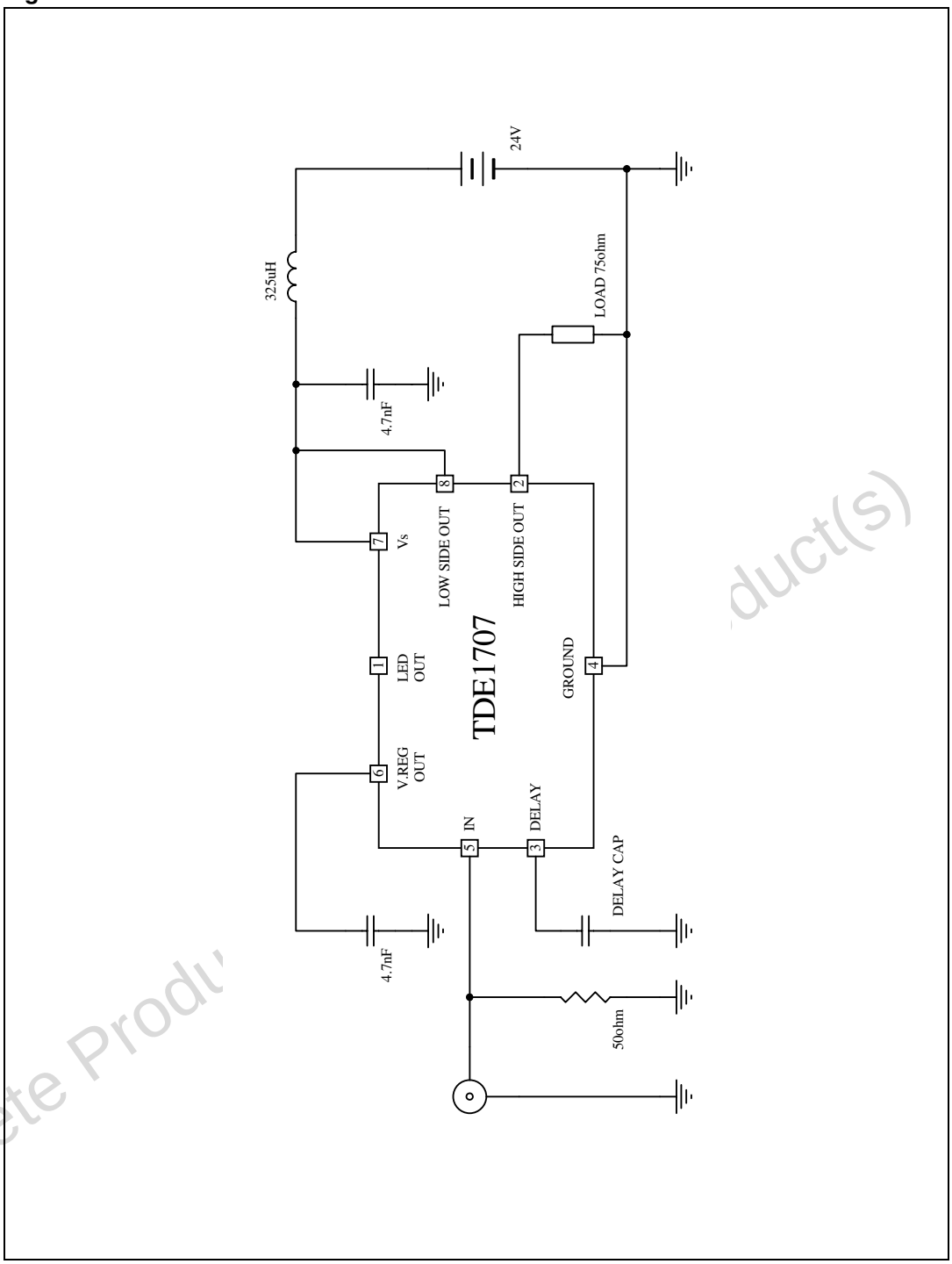

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Figure 3. Voltage on Vs and Vreg without filter capacitor

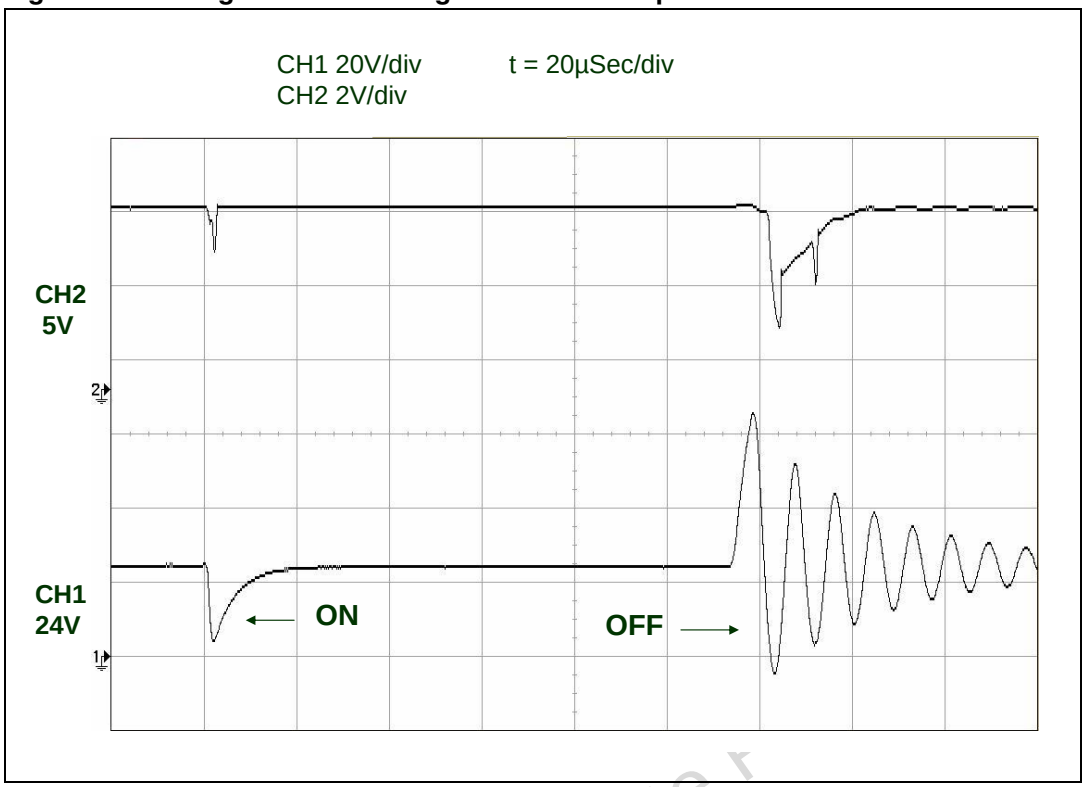
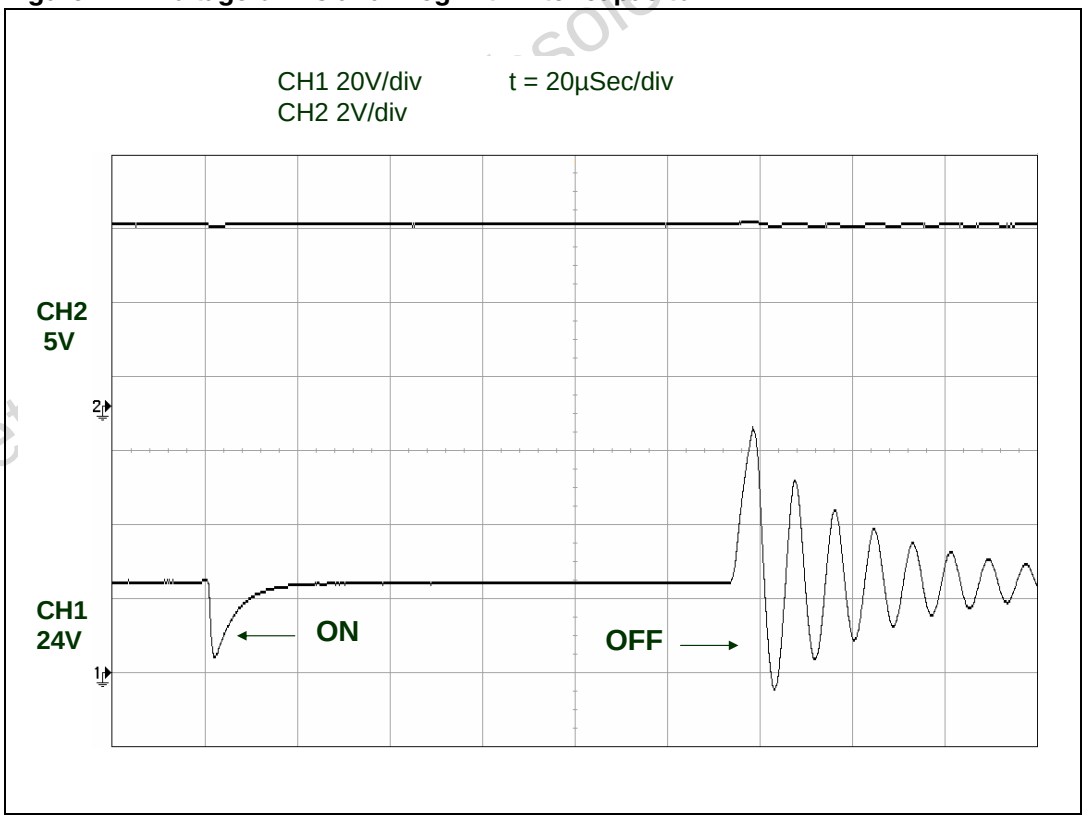


Figure 4. Voltage on Vs and Vreg with filter capacitor



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2 Revision history

Table 1. Revision history

Date	Revision	Changes
Nov-2003	1	First issue
14-Sep-2005	2	New template, no content change
14-Dec-2006	3	The document has been reformatted

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